DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirade, Junji et al (JP 02249333), hereinafter referred to as Hirade. A translated copy has been included in this Office Action.

Re claim 1: Hirade teaches a data processing apparatus adapted for performing scramble processing of transmit data (page 3: lines 1-2 of section "Problems to be solved by the invention") the data processing apparatus comprising:

scramble operation processing means including plural stages of shift registers (page 4: lines 1-4 of section "Means to solve the problems"), and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the transmit data to generate scramble-processed data (page 4: lines 6-9 and lines 12-13 of section "means to solve the problems"), and to sequentially input the scramble-processed data to the input stage of the shift register (page 9, lines 3-6);

data generating means for generating bit data of a predetermined pattern (page 4: line 4 of section "Means to solve the problems;" page 5, lines 1-3 of section "Operation"); and

switching means supplied with the scramble-processed data and the bit data of the predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data (page 6: lines 3-5 of section "Application examples;" page 8, lines 3-5), and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data (page 7, lines 1-7).

Re claim 2: Hirade teaches the data generating means is caused to be of the configuration to load the bit data of the predetermined pattern into the shift register at the time of synchronization processing of transmit data (page 5: lines 8-11 of section "Operation;" page 6, lines 3-15).

Re claim 5: Hirade teaches a data processing apparatus adapted for performing scramble processing of transmit data (page 3: lines 1-2 of section "Problems to be solved by the invention"), the data processing apparatus comprising:

cyclic code generating means for generating cyclic bit data train of a predetermined period (page 4: lines 6-9 and lines 12-13 of section "means to solve the problems" and page 5: lines 1-3 of section "Operation"),

EXOR operation means for sequentially performing EXOR operation of the cyclic bit data train with respect to the transmit data to output scramble-processed data (page 6, line 10 through page 7, line 7);

data generating means for generating bit data of a predetermined pattern (page 4: line 4 of section "Means to solve the problems;" page 5, lines 1-3 of section "Operation"); and

switching means supplied with the scramble-processed data and bit data of a predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data (page 6: lines 3-5 of section "Application examples;" page 8, lines 3-5), and to select the scramble-processed data when synchronization processing of the transmit data is not performed to output the data thus selected as scrambler output data (page 7, lines 1-7).

Re claims 3 and 6: Hirade teaches the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data (page 5: lines 8-11 of section "Operation;" page 6, lines 3-15).

Re claims 4 and 7: Hirade teaches the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance (page 3-4, entire section: "problems to be solved by the invention").

Re claim 8: Hirade teaches a data reception processing apparatus adapted for performing descramble processing of receive data (page 5, line 1; Fig 2: page 8, lines 6-8),

the data reception processing apparatus comprising: detecting means for detecting bit data of a predetermined pattern for synchronization from the receive data (page 8, lines 9-12; page 8, line 22 – page 9, line 2); and

descramble operation processing means including plural stages of shift registers, and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the receive data to output descramble-processed data (page 9, lines 3-6), and to sequentially input the descramble-processed data to the input stage of the shift registers (page 5, lines 1-10),

wherein the detecting means is caused to be of the configuration in which in the case where the bit data of the predetermined pattern is detected, the detecting means loads the bit data of the predetermined pattern into the shift register (page 5, lines 1-3 of section "Operation;" page 7, lines 3-5; page 8, lines 6-8).

Re claim 9: Hirade teaches the detecting means is caused to be of the configuration to specify information assigned in advance to the bit data of the predetermined pattern (page 3-4, entire section: "problems to be solved by the invention").

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat 5195136 A

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DARREN SCHWARTZ whose telephone number is (571)270-3850. The examiner can normally be reached on 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571)272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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